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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,264	01/11/2002	Satoshi Inaba	P 284163 01F181	6258

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,264	INABA, SATOSHI	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/13/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,47 and 48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *48* is/are allowed.

6)☒ Claim(s) *1-5,7,9-11 and 47* is/are rejected.

7)☒ Claim(s) *6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statements.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/13/2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,4,5,7,11, and 47 are rejected under 35 U.S.C. 102(b) as being anticipated by FUNAKI (5,463,237).

With regard to claim 47 Funaki discloses a semiconductor device comprising a semiconductor substrate having a surface; a gate electrode 25 formed over the surface of said semiconductor substrate with a gate dielectric film interposed therebetween; a

pair of source 22-27a and drain 23-27b diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode 25, said source 22-27a and drain 23-27b diffusion layers each having a low resistivity region 22-23 and an extension region 27a-b being formed to extend from this low resistivity region 22-23 toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region 22-23; a first impurity doped layer I of a first (p) conductivity type formed in said channel region between the source/drain diffusion layers; a second impurity doped layer II of a second conductivity type formed under said first impurity doped layer I; and a third impurity doped layer IV of the first (p) conductivity type formed under said second impurity doped layer II, and fourth impurity doped layers IIIa-b of the first (p) conductivity type embedded to be in contact with the extension regions 27a-b of said source 22-27a and drain 23-27b diffusion layers; wherein said three impurity doped layers I-II-IV make up a multilayer lamination structure with two p-n junctions, one between said first I and second II impurity doped layers and the other between said second and third impurity doped layer IV, wherein said first impurity doped layer I is equal to or less in junction depth than the extension region 27a-b of each of said source/drain diffusion layers, and wherein said second impurity doped layer II is determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said first I and third IV impurity

doped layers. Note figure 33, column 20 lines 53-67, and column 21 lines 41-42 of Funaki.

With regard to claims 1,4,5,7, and 11 Funaki discloses a semiconductor device comprising semiconductor substrate having a surface; a polysilicon film gate electrode 25 formed over the surface of said semiconductor substrate with a gate dielectric film interposed therebetween; a pair of source 22-27a and drain 23-27b diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode 25, said source 22-27a and drain 23-27b diffusion layers each having a low resistivity region 22-23 and an extension region 27a-b being formed to extend from this low resistivity region 22-23 toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region 22-23; a first impurity doped layer I of a first (p) conductivity type, said channel region (note column 21 lines 41-42) being formed in said first impurity doped layer I of a first (p) conductivity type between the source/drain diffusion layers; a second impurity doped layer II of a second conductivity type selectively formed in a region immediately beneath said gate electrode 25, under said first impurity doped layer I; and a third impurity doped layer IV of the first (p) conductivity type formed under said second impurity doped layer II, fourth impurity doped layers IIIa-b of the first (p) conductivity type embedded to be in contact with the extension regions 27a-b of said source 22-27a and drain 23-27b diffusion layers; wherein said three impurity doped layers I-II-IV make up a multilayer lamination

structure with two p-n junctions, one between said first I and second II impurity doped layers and the other between said second and third impurity doped layer IV, wherein said first impurity doped layer I is equal to or less in junction depth than the extension region 27a-b of each of said source/drain diffusion layers, and wherein said second impurity doped layer II is determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said first I and third IV impurity doped layers. Note figure 33, column 20 lines 53-67, and column 21 lines 41-42 of Funaki.

The applicant's claims 4 does not distinguish over the Funaki reference regardless of the process used to form the first and second impurity doped layers, because only the final product is relevant, not the recited process of forming said layers into an undoped semiconductor layer as has been epitaxially grown.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in

"product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1-3,5, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over MIYAMOTO et al. (5,675,172).

Miyamoto et al. discloses a semiconductor device comprising a semiconductor substrate 15 having a surface; a polysilicon film gate electrode 3 formed over the surface of said semiconductor substrate 15 with a gate dielectric film 10 interposed therebetween; a pair of source 4a and drain 4b-13 diffusion layers formed in said semiconductor substrate 15 to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode 3, said drain 4b-13 diffusion layer having a low resistivity region 4b and an extension region 13 being formed to extend from this low resistivity region 4b toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region 4b; a first impurity doped layer 5 of a first (p) conductivity type, said channel region being formed in said first impurity doped layer 5 of a first (p) conductivity type

between the source 4a/drain 4b-13 diffusion layers; a second impurity doped layer 6 of a second (n) conductivity type selectively formed in a region immediately beneath said gate electrode 3, formed under said first impurity doped layer 5; and a third impurity doped layer 7 of the first (p) conductivity type formed under said second impurity doped layer 6; wherein said three impurity doped layers 5-6-7 make up a multilayer lamination structure with two p-n junctions, one between said first 5 and second 6 impurity doped layers and the other between said second 6 and third 7 impurity doped layer, said first impurity doped layer 5 is equal to or less in junction depth than the extension region of each of said source 4a/drain 4b-13 diffusion layers, said second impurity doped layer 6 is determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said first 5 and third 7 impurity doped layers and said first impurity doped layer 5 is set in impurity concentration and thickness to be at least partially depleted, and in fact fully depleted, upon formation of a channel inversion layer. Note figure 10 and column 13 lines 12-50 of Miyamoto et al. Miyamoto et al. does not disclose that both said source 4a and drain 4b-13 diffusion layers each have a low resistivity region and an extension region being formed to extend from this low resistivity region toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region, disclosing rather only an extension region 13 for the drain 4b-13. However, it is well known that in practical circuit design using n-channel MOSFETs of the sort shown in Miyamoto's figure 10, sometimes it can be predicted that the designed circuit will always bias the

drain higher than the source, so that only the drain-channel junction need to be protected against breakdown by an extension region formed to extend from a low resistivity drain region toward the channel region and being lower in impurity concentration and shallower in depth than the low resistivity drain region, but that in some circuit designs it cannot be predicted which of the drain or source will be biased higher, in which case it is prudent to protect both the source and drain with such an extension region. Therefore, it would have been obvious to a person having skill in the art to augment the semiconductor device of Miyamoto et al. with extension regions formed on both source and drain regions in order to protect the semiconductor device against possible breakdowns due to the source being biased higher than the drain to thus provide a semiconductor device that is better protected against possibly catastrophic breakdown events.

B. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over MIYAMOTO et al. (5,675,172), as applied to claim 1, and further in view of CHEEK et al. (6,162,694).

Miyamoto et al. discloses a semiconductor device with all the limitations of claims 9 and 10 except that the gate electrode is formed of a metal film as contacted with the gate electrode film. Note figure 10 and column 13 lines 12-50 of Miyamoto et al. However, Cheek et al. discloses a method for replacing polysilicon gate electrodes with metal gate electrodes. Note figure 1 of Cheek et al. Therefore, it would have been obvious to a person having skill in the art to replace the polysilicon gate electrodes of

Miyamoto et al.'s semiconductor device with the metal gate electrodes such as taught by Cheek et al. in order to reduce the conductivity and increase the electric field of the gate electrodes to thus provide a faster and more compact semiconductor device.

Allowable Subject Matter

4. Claims 6 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claim 48 is allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device comprising a semiconductor substrate having a surface; a gate electrode formed over the surface of said semiconductor substrate with a gate dielectric film interposed therebetween; a pair of source and drain diffusion layers formed in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate electrode, said source and drain diffusion layers each having a low resistivity region and an extension region being formed to extend from this low resistivity region toward said channel region and being lower in impurity concentration and shallower in depth than said low resistivity region; a first impurity doped layer of a first conductivity type formed in said channel region between the source/drain diffusion layers; a second impurity doped layer of a second conductivity type formed under said first impurity doped layer; and a third impurity doped layer of the

first conductivity type formed under said second impurity doped layer, wherein said three impurity doped layers make up a multilayer lamination structure with two p-n junctions, one between said first and second impurity doped layers and the other between said second and third impurity doped layer, wherein said first impurity doped layer is equal to or less in junction depth than the extension region of each of said source/drain diffusion layers, and wherein said second impurity doped layer is determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said first and third impurity doped layers, and wherein the low resistivity regions of said source/drain diffusion layers are formed to have top surfaces higher in level than said gate dielectric film, as recited in claim 48.

Response to Arguments

6. Applicant's arguments with respect to claims 1-5,7,9-11, and 47 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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